Application Note

High-Frequency, Over-Temperature Measurements and Modeling

Abstract

Recent advances in thermal probing equipment have dramatically reduced the cost of obtaining temperature-dependent S-parameter data, while increasing throughput capabilities. These advances have made thermal device modeling and process characterization practical and affordable. However, the extreme range in temperatures of interest, –65° C to 200” C, has increased the complexity of the calibration and measurement considerations. An overview of the ECP (equivalent circuit parameter) extraction method, thermal probing system configuration, calibration considerations, and measurement issues is presented. General extraction results are shown for MESFET, PHEMT, and HBT devices.

Introduction

Airborne and space-based electronic systems have always demanded high-frequency integrated circuits which perform well in wide-ranging thermal environments. The success of newly emerging personal communications systems relies in part on the ability to inexpensively manufacture high-performance, high-yield integrated circuits (ICs) which function in demanding thermal environments. To accomplish this, designers require more physically-meaningful device models as well as a greater understanding of their semiconductor material processes.

However, traditional methods used for testing these ICs over-temperature are both costly and inefficient. New low-cost and high-throughput, on-wafer temperature testing methods must be employed to obtain the necessary data. This data can then be analyzed with improved ECP (equivalent circuit parameter) extraction techniques, such as those employing cold-FET, pinched-FET, and hot-FET S-parameter measurements, to generate accurate temperature and bias-dependent device models.

General Extraction Method

Currently, the extraction methods most commonly used for temperature and bias-dependent device modeling use some combination of cold-FET, pinched-FET, and hot-FET S-parameter measurements over temperature. Research by Dambrine et.al.[1], Berroth and Bosch[2], and Anholt and Swirhun[3] proposes that such measurements uniquely determine the device ECPs, unlike brute force optimization methods used previously. Figure 1 illustrates the conventional small-signal MESFET equivalent circuit model. The physical origin of these equivalent circuit parameters is shown in Figure 2. In most cases, the extracted ECPs can be fit to a linear temperature dependence:

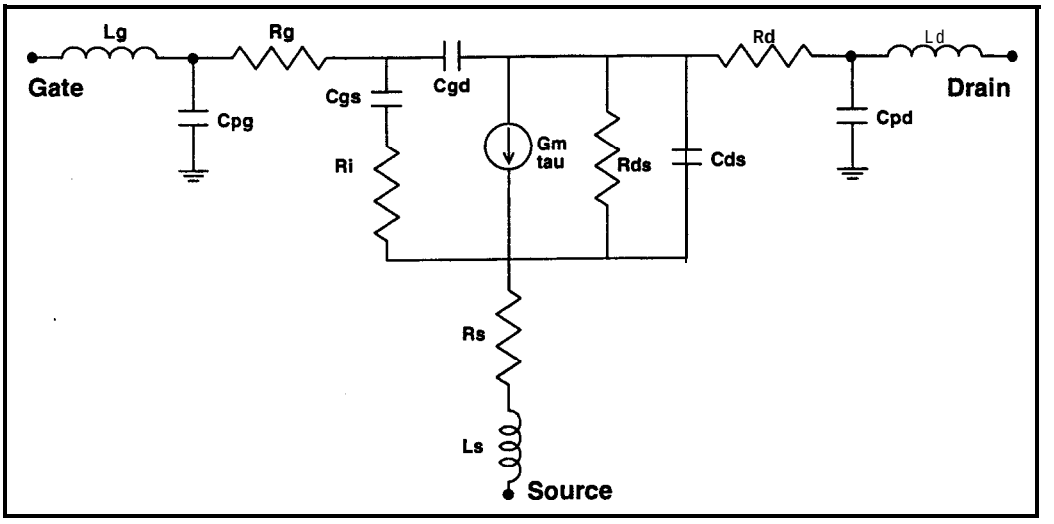


Figure 1. Conventional small-signal MESFET topology.

$$ECP(V_g, V_{ds}, T) = ECP(V_g, V_{ds}, T_o)[1 + B(V_g, V_{ds})(T - T_o)]$$

where T_o = 300K and B is the temperature coefficient for a given ECP, usually expressed in parts per thousand.

The cold-FET condition implies a strong forward bias applied to the gate with V_{ds} = OV. S-parameter measurements made under these conditions extract the extrinsic, or parasitic, circuit elements. Under forward gate bias, the FET effectively becomes a two-terminal device. Figure 3 shows the equivalent circuit for the cold-FET bias condition, in which the FET effectively represents a distributed Schottky diode[4]. S-parameters are typically measured under three of four different forward bias conditions. These S-parameters are then converted to Z-parameters. The $Re[Z_{11}]$ is plotted vs. $1/I_g$, and the curve is extrapolated back to the origin to obtain the sum $(R_s + R_g)$. R_s, R_d, and R_g can then be obtained from $Re[Z_{21}]$, $Re[Z_{22}]$, and $Re[Z_{11}]$ respectively. Once the extrinsic circuit elements have been determined, the hot-FET bias measurements are used

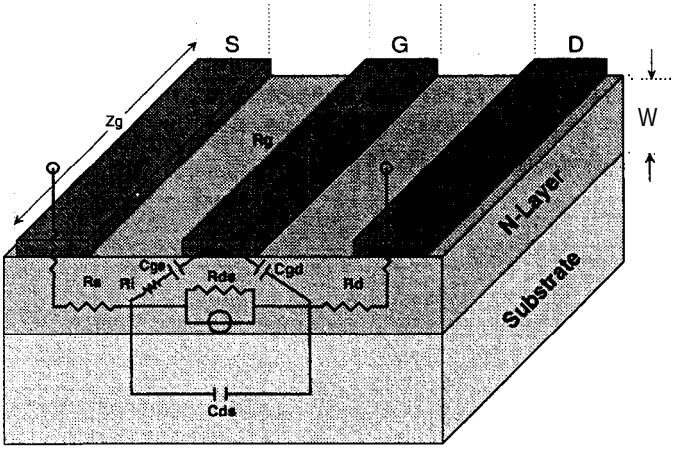


Figure 2. Basic MESFET dimensions and physical origin of equivalent circuit parameters.

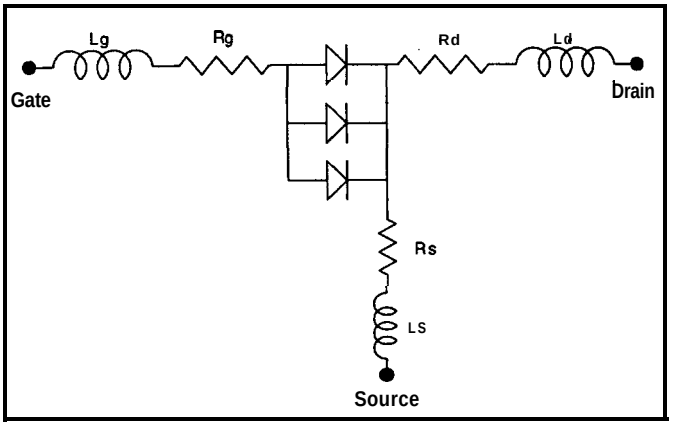


Figure 3. MESFET equivalent circuit in cold-FET configuration.

to extract the intrinsic circuit elements. Hot-FET bias implies a typical amplifier operating bias point, $V_{gs} < OV$ and $V_{ds} > OV$. Data is commonly taken for one hundred or more bias points at each temperature.

Extrinsic circuit elements: $R_g, R_d, R_s, L_g, L_d, L_s$

$$Z_{11} = R_s + R_g + nkT/qI_g + j(L_s + L_g) + (R_{ch}/3)$$
$$Z_{22} = R_s + R_d + j(L_s + L_d) + R_{ch}$$
$$Z_{21} = Z_{12} = R_s + jL_s + (R_{ch}/2)$$

Intrinsic circuit elements: $g_m, R_{ds}, R_{in}, C_{gs}, C_{ds}, C_{gd}$

Finally, the pinched-FET measurements are used to determine the parasitic capacitances C_{pg} and C_{pd}. The pinched-FET condition implies V_{ds} = OV and V_{gs} c Vp. According to Anholt and Swirhun, C_{pg} and C_{pd} result from "capacitance on the fringe of the gate in the semiconductor, inter-electrode capacitance over the top of the semiconductor, and pad capacitance associated with the measurement."[5] These parasitic capacitances may be quite significant when measuring small gate-width and small gate-length devices. Figure 4 shows the equivalent circuit for the pinched FET. Since C_{gs}' and C_{gd}' are approximately equal under these conditions, C_{pg} and C_{pd} can be determined from $Im_{[Y11]}$ and $Im_{[Y22]}$ respectively.

$$C_{gs}' = C_{gd}' = C'$$

$$Im_{[Y11]} = j(C_{pg} + 2C')$$
$$Im_{[Y22]} = j(C_{pd} + C')$$
$$Im_{[Y21]} = Im_{[Y12]} = -jC'$$

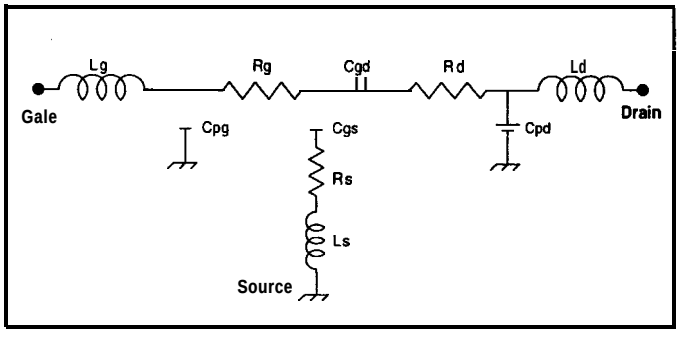


Figure 4. Pinched-FET equivalent circuit.

Thermal Probing System Configuration

The goal of temperature modeling is to accurately describe the RF device behavior for a given semiconductor material process. This activity requires a large number of test samples to ensure confidence. Traditionally, designers have mounted discrete devices or MMIC chips on carriers, placed these carriers in test fixtures, and then cycled them over temperature. This is a tedious and costly procedure that requires custom test fixtures, awkward test set-ups, and a great deal of labor. Test fixtures plague measurements with inaccuracies due to ground problems, bias oscillations, and reflective transitions. Because of the low throughput, it has never been practical to test enough devices to adequately characterize the RF performance over temperature for a foundry's material process -or for even a single wafer.

The most practical and economical implementation of temperature testing is at the wafer level. Until recently, on-wafer testing over temperature required custom systems configured with an assortment of probe stations, dry boxes, probes, and cable components. The entire probe station is enclosed in the dry box, with electrical connections brought in through sealed ports. Glove ports in the dry box wall are used to handle the wafer and to manipulate the probe station and positioners. The dry box is purged with dry nitrogen to avoid frost at low temperatures[6]. Purging this large volume is time consuming and often requires several hours. In general, these systems are expensive, provide poor throughput, and are quite awkward to use. They also make calibration issues over temperature difficult to address.

To solve both throughput and accuracy problems, Cascade Microtech has developed a compact, integrated and economical alternative for obtaining temperature-dependent S-parameter data. Figure 5 shows this thermal parametric probe station with an HP8510 network analyzer. The probe station's features include:

- Dry, frost-free probing environment with fast purge time
- Dark, EMI-isolated enclosure that reduces measurement uncertainty
- Fast, accurate, stable wafer heating and cooling (-65" C to +200° C)
- Limited electrical drift of calibration standards, probes, and cables over temperature
- Compensation capability for wafer expansion (TCE)

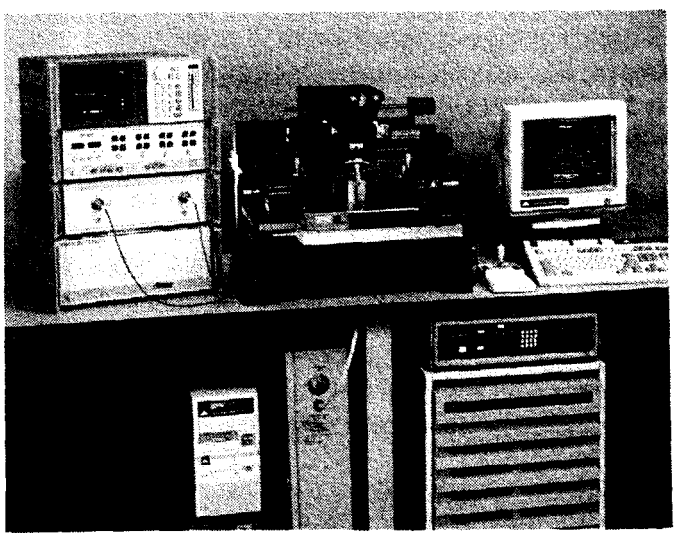


Figure 5. Cascade Microtech semi-automatic thermal probe station.

The Cascade Microtech system features the MicroChamber™ (Figure 6), which serves the same purpose as an entire dry box, without surrounding the entire station. The MicroChamber encloses the thermal chuck and probing area in a 7.0 liter volume, which reduces purge times to less than 15 minutes and also minimizes temperature-related electrical drift caused by heating and cooling of the probes and cables. The MicroChamber contains two calibration substrate stages that are thermally isolated to minimize variations in the impedance standards.

The MicroChamber shields the wafer under test from ambient air, light, and electromagnetic interference (EMI). An integrated temperature controller and air dryer provide the dry and stable thermal environment within the MicroChamber. As Figure 7 illustrates, the chuck transitions from room temperature to -65" C or to +200° C in a matter of minutes.



Figure 5. Close-up of the MicroChamber, found on both manual and semi-automatic systems.

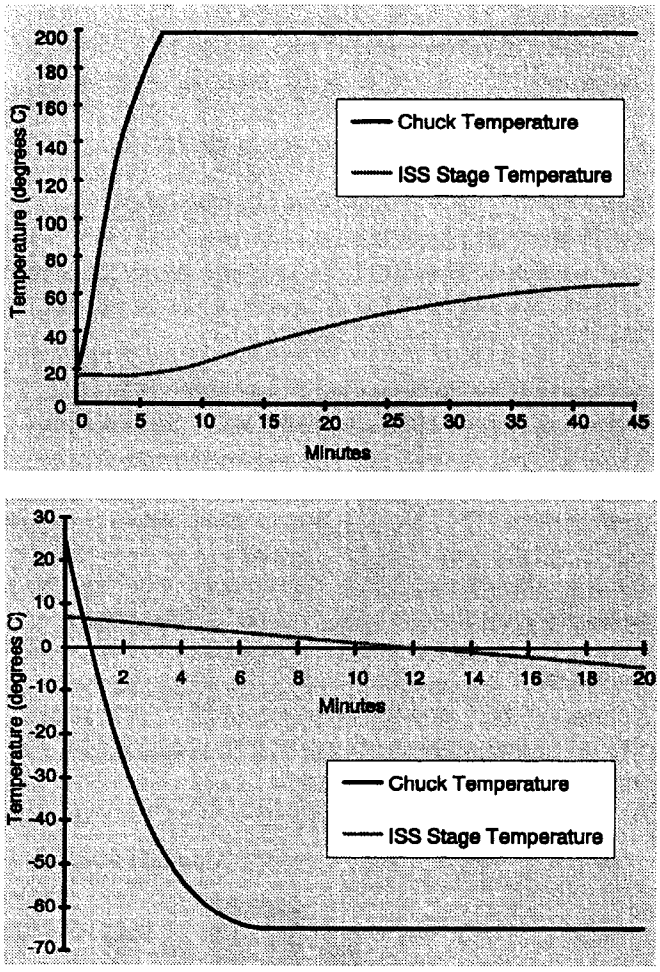


Figure 7. Transition times for system.

Calibration and Measurement Issues

Calibration stability and measurement accuracy over temperature are the most important (and most often neglected) thermal probing issues. Cascade Microtech's thermal probing system addresses these key issues. The system offers optional VNA calibration software that automatically performs LRRM (line-reflect-reflect-match) or SOLT (short-open-load-thru) calibrations and displays a calibration verification plot, shown in Figure 8. A calibration verification plot which exceeds 0.1 dB may indicate loose connections or non-planar probes. A separate calibration stability check measures changes in the system over time and/or temperature since the last calibration was performed. The software measures and displays the vector difference between an open circuit probe measurement and the original open calibration data (Figure 9). The initial calibration stability should be greater than -60dB or 0.1%. A new calibration should be performed whenever the stability reaches -4OdB or 1%. Calibration stability is affected by the following factors:

- Instrument variations over time
- Probe placement errors resulting from thermal expansion of the wafer chuck
- Changes in the calibration standards with temperature
- Electrical drift because of probe and cable temperature variations

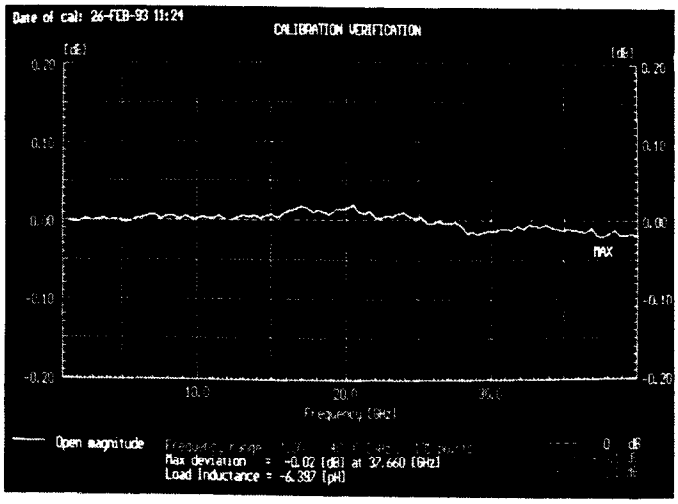


Figure 8. Typical calibration verification plot.

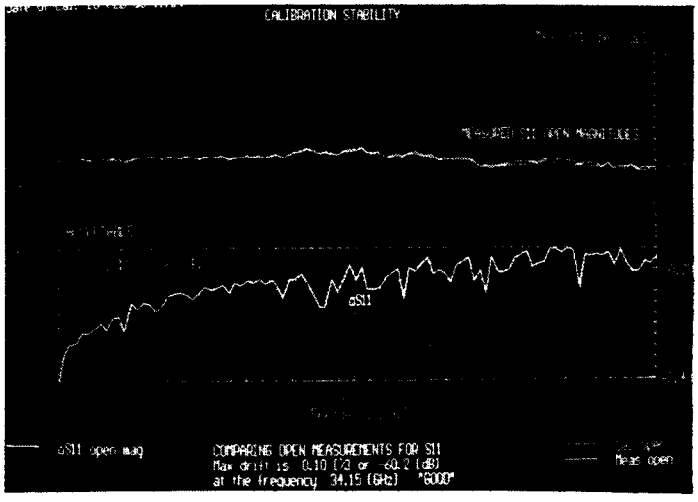


Figure 9. Typical calibration stability plot.

Instrument variations over time are always an issue, even in room temperature measurements. To ensure the integrity of the measurements, a calibration stability check should be performed every hour.

As the chuck changes temperature, it expands and contracts, affecting the over-travel of the probes. Figure 10 shows typical thermal expansion characteristics of the thermal chuck. The total expansion of the chuck from –65° C to +200° C is about 9 mils. The overtravel of the probe tips must be readjusted at each temperature.

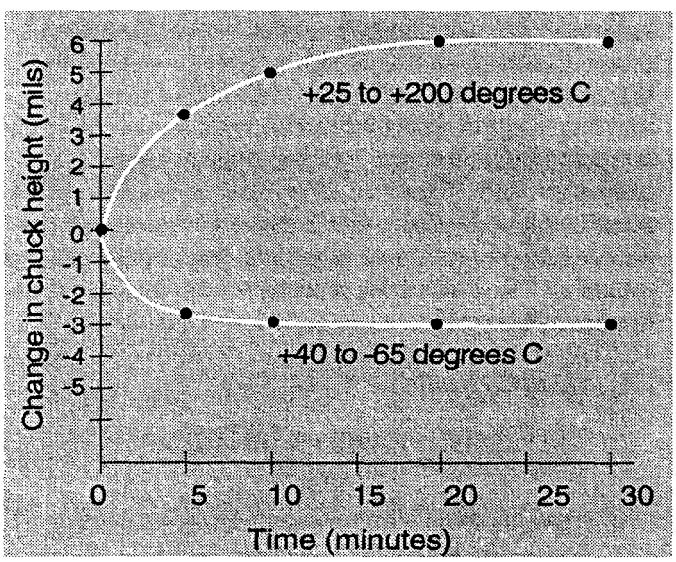


Figure 10. Typical thermal chuck vertical expansion/contraction.

Probe placement problems on the wafer can affect measurement accuracy, especially at frequencies above 40 GHz. The diameter of the wafer changes with temperature, resulting in small spacing changes between devices. Cascade's semi-automatic thermal probe station provides automatic compensation for these effects, minimizing the impact on measurement accuracy.

Changes in the calibration standards, probes,and cables are often erroneously ignored. In general, LRM, LRRM, SOLT, and TRL calibrations can all be used for over temperature measurements. However, the implementation of the standards can greatly affect their accuracy. For example, variations in the dielectric constant of the substrate material, via hole integrity, or changes in the load/match standard with temperature must be considered. The primary consideration with LRM or LRRM standards is the sensitivity of the 50-ohm load standard to temperature variations. The thermally-isolated calibration chuck described above was designed to minimize the temperature variation of this load by reducing the temperature excursions of the calibration substrate. As shown in Figure 7, a main chuck temperature range of –65° C to +200° C represents a temperature range of about +5° C to +65° C for the isolated chuck. This smaller temperature excursion reduces the total variation in the load resistance to about 0.7%. LRM standards fabricated on-wafer will have greater variations, perhaps as large as 3%.

To illustrate the likely impact of improper calibration, over-temperature measurements were performed on MESFET and PHEMT wafers. Approximately 20 devices were probed on each wafer at cold-FET, hot-FET, and pinched-FET bias conditions. From these measurements, ECPs were directly extracted. For each device, the temperature coefficient (TC) of each ECP was computed from the T = 20°C to T = 125°C differences. Figure 11 shows the results for the MESFET wafer. For the hot-FET g_m (approximately 50% Idss), the average TC was -1 .5E^{-3} and the error was .02E^{-3}, or less than 2%. At room temperature, g_m at 50% Idss for both wafers had less than 2% variation.'

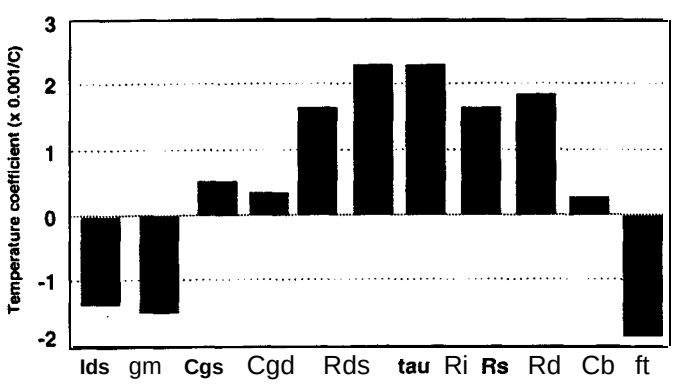


Figure 11. Temperature coefficients for 0.5 x 150-µm MESFET.

Figure 12 shows the PHEMT results. This figure compares the extracted TCs from measurements made with two different calibrations: cold-cal and hot-cal. Cold-cal refers to a calibration performed on standards located on Cascade's isolated thermal chuck. This chuck typically stays at 40°C while the main chuck is at 125°C. Hot-cal refers to calibrations made on the main thermal chuck. The TC for g_m was determined to be –1.2E^{-3} for the cold-cal, while the hot-cal resulted in a TC of -1 .3E^{-3}. This differ-

ence is the result of the variation in the 50-ohm match standard, which has drifted to approximately 50.5 ohms at 125°C. The error introduced by the hot-cal was determined by comparing the extracted cold-cal and hot-cal TCs. Figure 12 shows that this error is as large, or larger, than the statistical error in the TCs for many of the parameters.

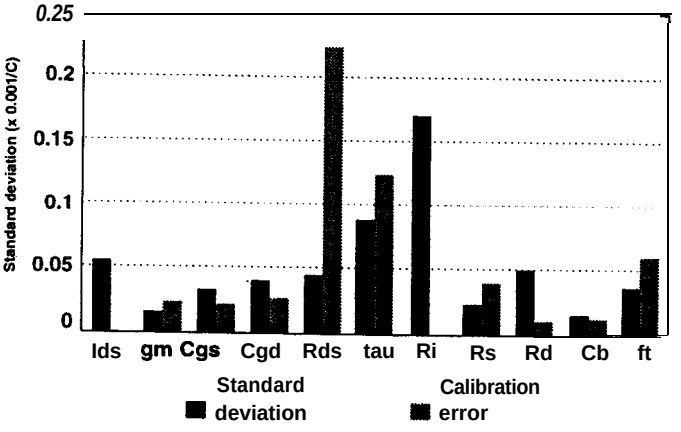


Figure 12. Standard deviations of temperature coefficients compared with calibration errors.

Changes in the probes and cables can have great impact on calibration and measurement accuracy. A typical wafer probe thermal profile is shown in Figure 13. With a chuck temperature of +200° C, the associated coaxial connector temperature is about +75° C. Since the probes are in direct contact with the substrate, the coax connector and coax-to-coplanar transition experience significant thermal changes. Experiments have shown that these changes are large enough to require new calibrations at each temperature.

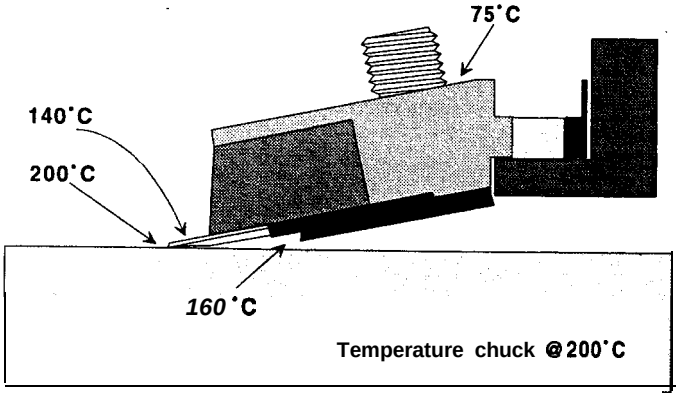


Figure 13. Temperature readings across WPH-Series probe.

Figure 14 illustrates the changes observed in calibration stability for a room temperature calibration after the chuck transitions to +200° C. The calibration stability is clearly unacceptable. Note that the probe is still changing during the first 15 minutes. For optimal results, a 15-minute probe stabilization period is required at each temperature. Since the expansion of the probe board represents a larger fraction of a wavelength at higher frequencies, the calibration stability exhibits greater degradation with increasing frequency. Thermal stability of the probe is both a calibration issue and a measurement issue. The probe temperature should be the same for both the calibration and the measurement.*

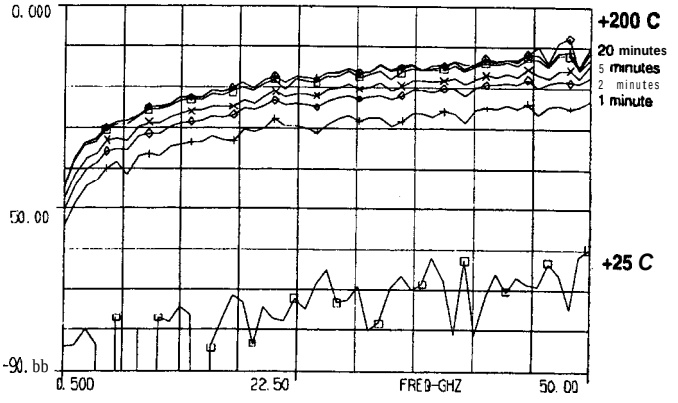


Figure 14. Calibration stability at 200° C for a 25° C calibration.

In addition to the probe temperature, other measurement issues must be considered. These include RF power levels, resistive loss in the bias lines, and device stability. At low temperatures, the device gain can increase considerably. The RF power levels to the device should be adjusted to ensure linear operation over the entire temperature range. A simple test for a bias dependent device model is to verify that it replicates the DC family of curves measured on a curve tracer. While the resistive losses in the bias lines do not affect the RF measurements, the DC bias point may be significantly different at the device. This is especially true for higher current devices. Unless these resistive losses are accounted for, the curve tracer data may not agree with the extracted bias dependent model. Finally, device stability must be considered. Because of the potentially high gain at low temperatures, some devices may have a tendency to oscillate. Precautions must be taken to ensure stability. Cascade Microtech suggests following the measurement sequence shown in Figure 15.

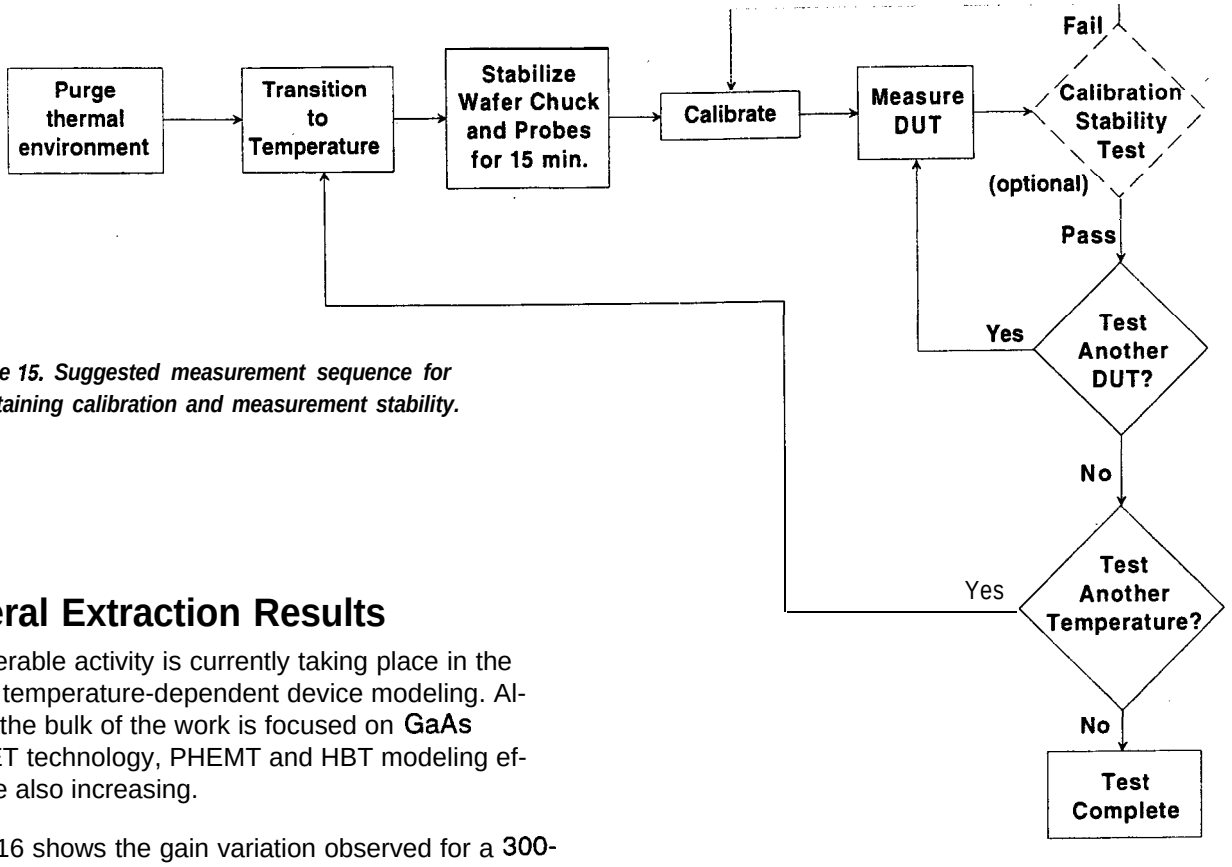


Figure 15. Suggested measurement sequence for maintaining calibration and measurement stability.

General Extraction Results

Considerable activity is currently taking place in the area of temperature-dependent device modeling. Although the bulk of the work is focused on GaAs MESFET technology, PHEMT and HBT modeling efforts are also increasing.

Figure 16 shows the gain variation observed for a 300-micron gate-width GaAs MESFET over a -50” C to +125° C temperature range. As expected, the gain is higher at lower temperatures.

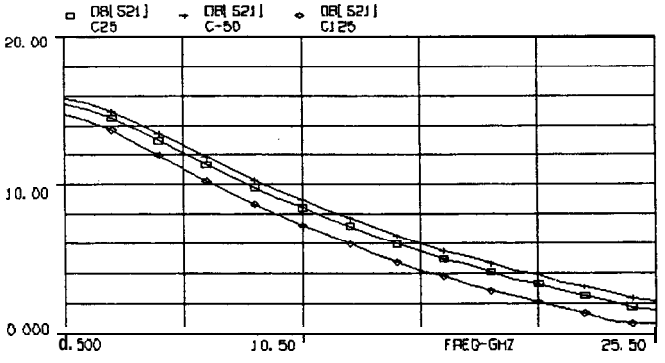


Figure 16. Gain variation from –50° C to +125° C.

Figure 17 shows the changes observed in S_{22} for this device over temperature. The bias conditions for these measurements were V_{gs} = OV and V_{ds} = 2.0V.

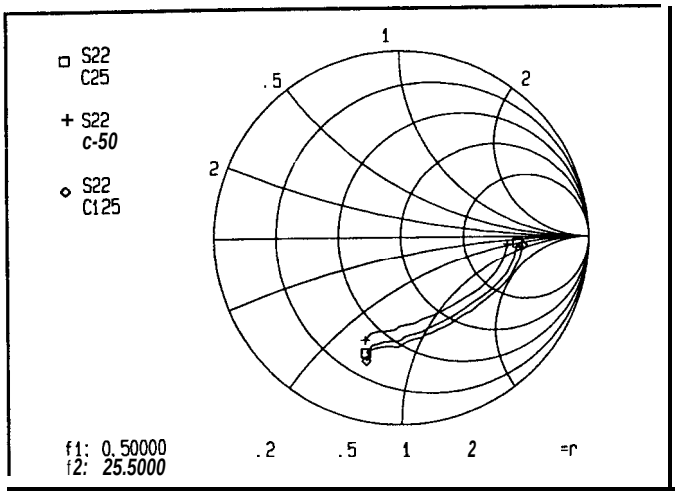


Figure 17. S_{22} from –50° C to +125° C.

Figures 18 and 19 illustrate typical 25° C cold-FET and pinched-FET data respectively.

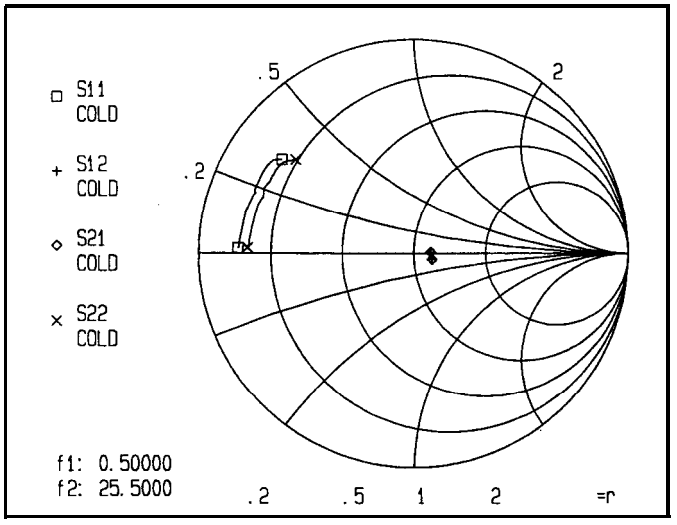


Figure 18. 25°C cold-FET measurement.

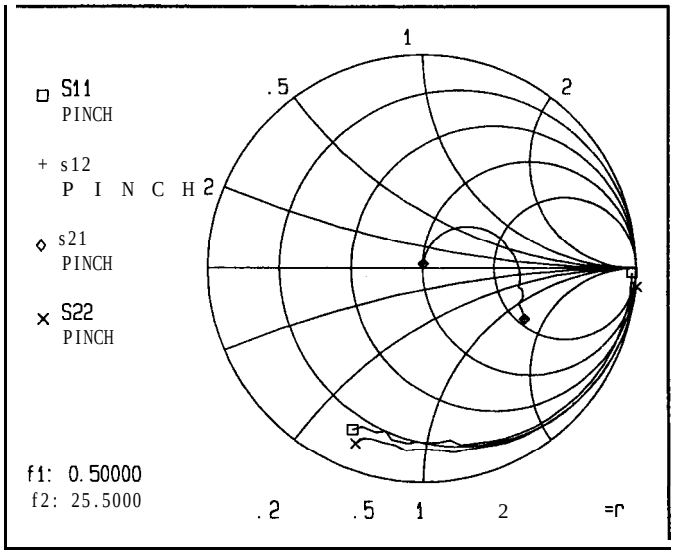


Figure 79. 25°C ***pinched-FET measurement.***

Sample extracted FET parameter data and temperature coefficients are shown in Table 1. Figures 20 and 21 plot two of these parameters, C_{gs} and transconductance (g_m), versus temperature.

Parameter	ECP	B (10^{-3}/°C)
g_m (ms)	38	-1.37
C_{gs} (fF)	181	0.12
C_{gd} (fF)	27	0.32
C_{ds} (fF)	69	0.23
f_t (GHz)	25	-1.23
τ (ps)	1.08	—
R_{ds} (Ω)	295	1.0
R_i (Ω)	6.0	—
R_g (Ω)	2.0	2.25
R_s (Ω)	2.44	0.92
R_d (Ω)	4.8	1.03
L_g (pH)	84	0.13
L_s (pH)	6.2	-0.15
L_d (pH)	92	< 0.1

Table 1. MESFET ECP data, V_{gs} = -1.0 V, V_{ds}=2.0V.

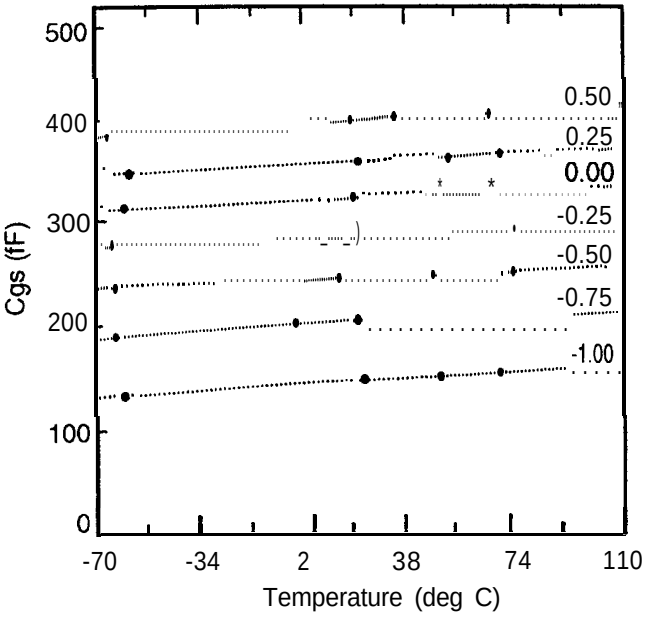


Figure 20. Cgs dependence over temperature.

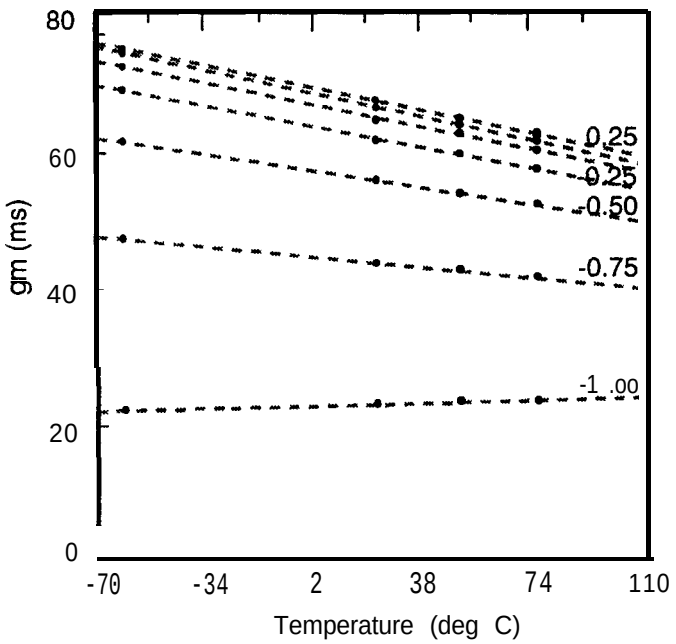


Figure 21. Transconductance (gm) temperature dependence

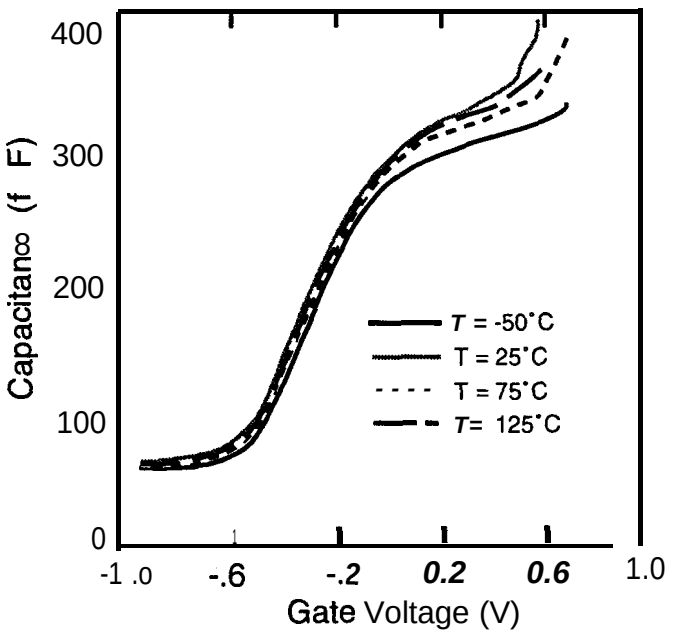


Figure 22. Capacitance vs. bias and temperature for a 200-µm PHEMT.

The temperature dependence of PHEMT ECPs are similar to those of the MESFET. The parameters for a 200- micron gate-width PHEMT are given in Table 2. Figures 22 and 23 show plots of capacitances and ft versus gate voltage and temperature.

Parameter	ECP	B (10^{-3}/°C)
g_m (ms)	150	-1.03
C_{gs} (fF)	276	0.31
C_{gd} (fF)	40	0.10
C_{ds} (fF)	48	0.10
f_t (GHz)	68	-1.43
τ (ps)	0.48	-0.64
R_{ds} (Ω)	154	0.46
R_g (Ω)	0.6	–
R_s (Ω)	1.6	1.47
R_d (Ω)	2.1	2.25

Table 2. PUEMT ECP data, V_{gs} = 0 V, V_{ds} = 2.0V.

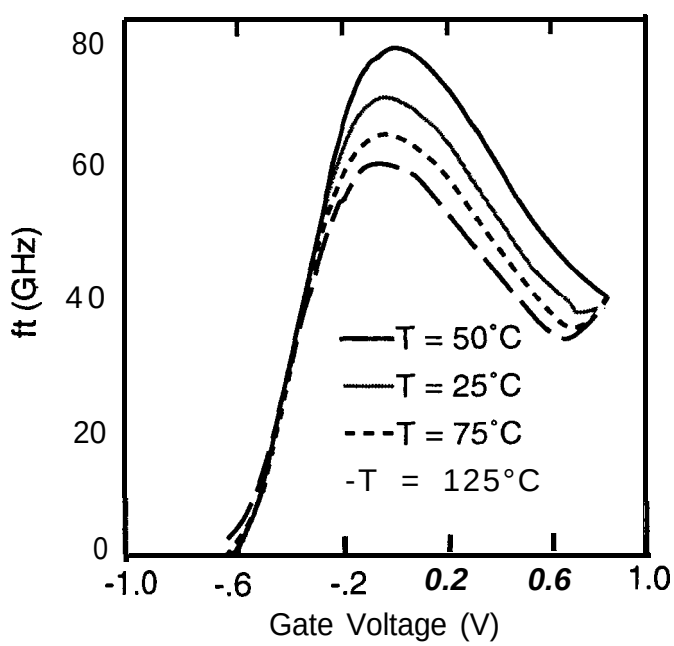


Figure 23. ft vs. bias and temperature for a 200-µm PHEMT.

The HBT extraction work is only just beginning. Figures 24 and 25 show some preliminary data for f_t versus Vbe and Ic.

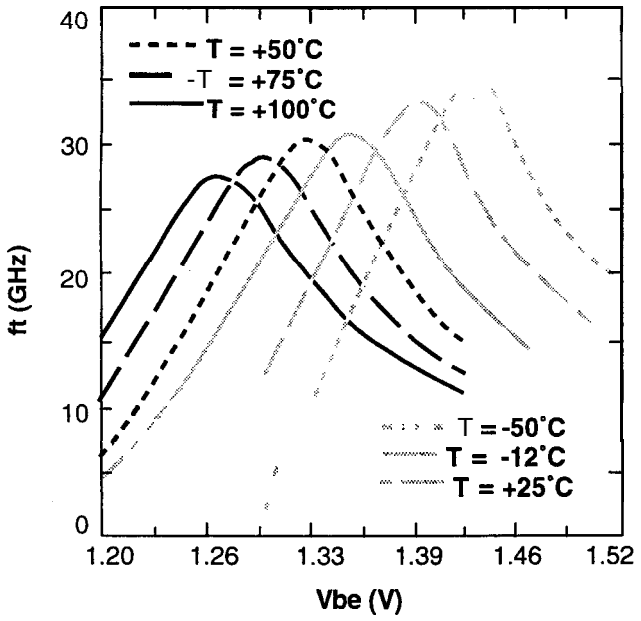


Figure 24. *HBT ft versus* V_{be}

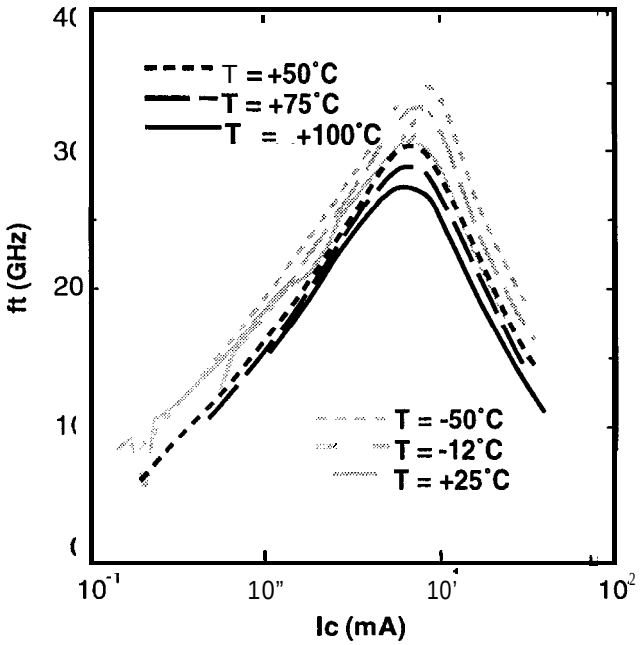


Figure 25. *HBT ft versus Ic.*

Figure 26 illustrates HBT junction capacitances over temperature.

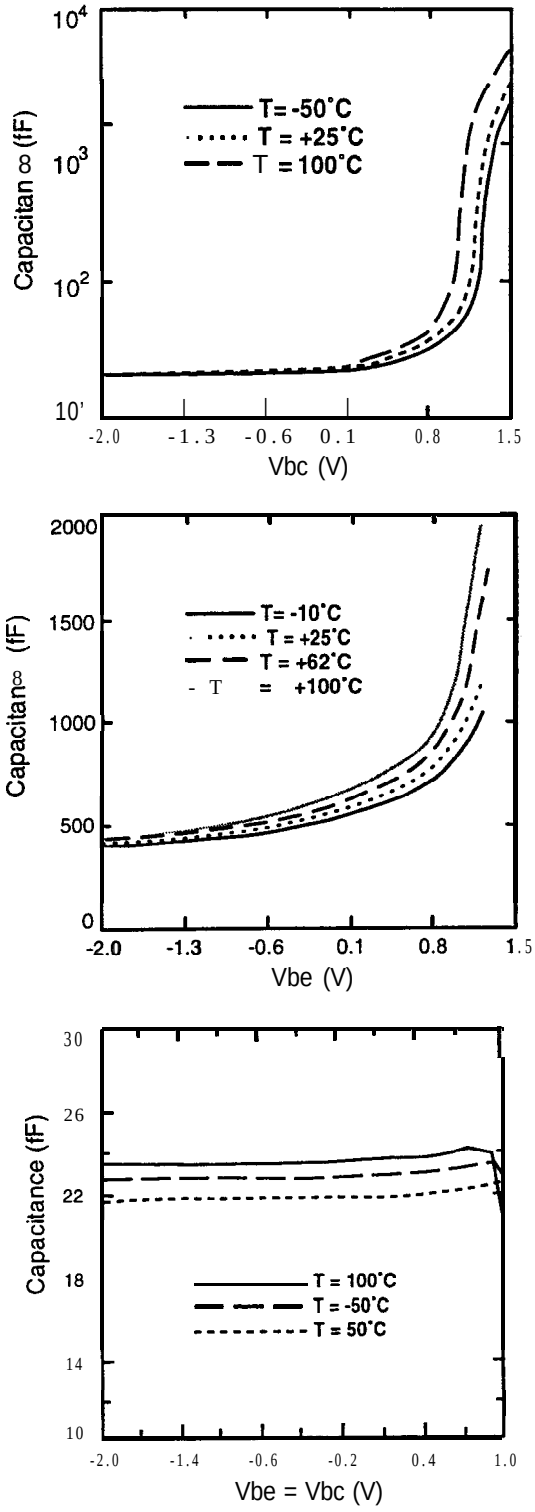


Figure 26. *HBT junction capacitances.*

Figures 27 and 28 show HBT base and emitter resistances respectively over temperature.

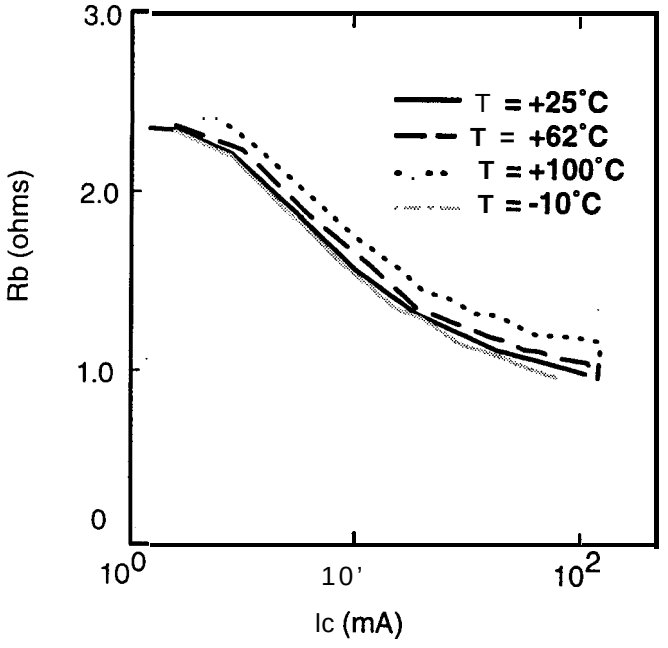


Figure 27. HBT base **resistances** *over temperature.*

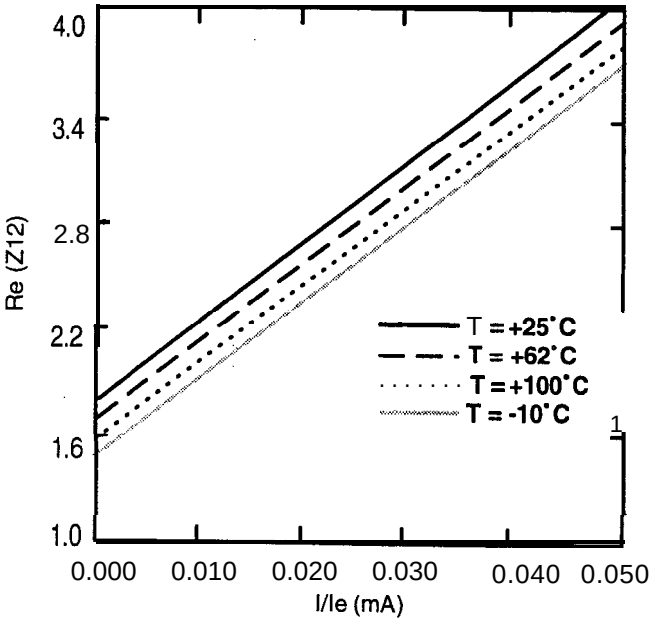


Figure 28. HBT emitter resistances over temperature.

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